REMARKS

This Amendment is responsive to the December 22, 2006 Office Action rejecting all pending claims 1-7 and 9-13. By this response claim 1 is amended and new claim 23 is added. Consideration and allowance of claims 1-7, 9-13 and 23 in view of the following remarks is requested.

§112 Rejection

Claims 1-7 and 9-13 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. In particular, the Office Action objected to features added to claim 1 by the October 10, 2006 Amendment reciting "to fill the aperture in the insulating layer with the first conductive material ... to a height about equal to or greater than the surface of the conductive lead layer." The Office Action asserts that this claim language suggests that the electroplated first conductive material over the aperture has a height equal to or greater than the surface of the conductive lead layer, but that there is no evidence in the application disclosure to support the amended limitations. Figure 6 is said to show that the electroplated first conductive material in the aperture is below the surface of the conductive lead layer.

By this response the phrase "having an upper surface" that referred to the conductive lead layer is deleted from claim 1. Also deleted from claim 1 is the phrase "fill the aperture in the insulating layer with the first conductive material." In view of these amendments it is believed that the basis for the rejection is now moot.

Attached as Exhibit 1 is a copy of Figure 6 marked with a red line extending between the unplated lower surface portions of the conductor layer (214) on opposite sides of the aperture (242). As is evident from this marked drawing, the height of the interconnect plating (246) in the center portion of the aperture exceeds the height of the red line. On the outer portion of the aperture, the height of the interconnect plating equals the height of the plated conductor layer. Attached as Exhibit 2 is a copy of Figure 11 marked with a red line extending between the unplated upper surface portions of the conductor layer (414) on opposite sides of the aperture (442). It is evident from this marked drawing that the height of

the interconnect plating (446) is at least equal to the height of the unplated conductor layer. These positions are also supported by the written specification. For these reasons amended claim 1 meets the requirements of §112, first paragraph. Withdrawal of the rejection is therefore requested.

§103 Rejection of Claims 1, 6, 7 and 9-11

Claims 1, 6, 7 and 9-11 stand rejected under 35 U.S.C. §103 as being unpatentable over the Cowles et al. U.S. Patent 6,700,748 in view of the Rinne et al. U.S. Patent 6,117,299. The Office Action asserts that the Cowles patent teaches a method for forming an electrical interconnect on an integrated suspension, but differs from the claims in that it does not explicitly teach filling the aperture to the height of the claim. The Rinne patent is relied upon as teaching electroplating an aperture in an insulating layer with a conductive material to the same thickness as the top surface layer. The position was taken that it would have been obvious to electroplate the conductive material to a height equal to the surface of the conductive lead layer because it would form a reliable interconnect. In connection with this position the Office Action asserts that the claim language is open to partial filling of the aperture, and that the teaching of the Cowles patent reads on the claim limitation.

The applicant respectfully disagrees with these positions. However, to more particularly point out and distinctly claim the invention, the applicant has by this amendment deleted the claim language regarding filling the aperture, and included other features to distinguish the invention from the prior art of record.

Specifically, with the amendments made to claim 1, claims 1, 7, 10 and 11 now recite the mask application step as including forming masked portions of the conductive lead layer or unmasked portions of the conductive lead layer at the interconnect site. The plated interconnect formed by the electroplating step has the physical structure of the conductive material as electroplated. Furthermore, during the building up of the first conductive material on the spring metal layer, the conductive material does not electroplate onto any unmasked portions of the conductive lead layer until the built up material reaches a thickness at which the conductive material contacts any unmasked portions of the conductive lead

layer at the interconnect site. This process is considerably different than that taught or suggested by the Cowles and Rinne patents.

The Cowles patent discloses a soldering process for forming an interconnect. As shown in the "Plated Solder" drawing in Figure 2, the solder is initially plated onto the exposed surfaces of *both* the stainless steel and copper layers in the via. Separate layers of solder are shown in the drawing over *both* the copper layer edge and the stainless steel surface in the via. The edges of these separate layers intersect near the outer edge of the stainless steel layer. This simultaneous electroplating on both the copper and stainless steel layers is consistent with the illustration of the voltage source "V" being connected between the copper and stainless steel layers. The fact that the layer of solder over the copper layer is thicker than the layer over the stainless steel layer may be caused by the fact that copper is a better conductor than stainless steel, and may therefore plate at a faster rate.

By the amendments made with this response, claim 1 now recites a process by which the conductive material of the interconnect will initially build up only on the spring metal layer (i.e., not on any masked or unmasked portions of the conductive lead layer at the interconnect site). With continued build up the conductive material will reach a height equal to or greater than the surface of the conductive lead layer. But unless there are unmasked portions of the conductive lead layer at the interconnect site, and even then only after the conductive material has built up to the thickness of the lead layer, the conductive material will not electroplate onto the conductive lead layer. This method enables the efficient fabrication of high-quality interconnects. It is also considerably different than the method disclosed in the Cowles patent, which involves simultaneously plating solder onto both the stainless steel and copper layers at the via.

Furthermore, the solder plating process shown in the Cowles patent is only an initial step in the overall ground path formation process. The plating step is done in the first instance to apply the solder to the via site. However, this initial plating step apparently does not produce an acceptable interconnect. As is evident from the drawing in Figure 2, the area of interconnection between solder plated on the stainless steel layer and the solder plated on the copper layer is relatively small, and may not form a satisfactory electrical connection.

The specification of the Cowles patent, in the sentence bridging columns 3 and 4, states that the solder is reflowed for increased adhesion to the underlying material. The ground connection after the solder reflow step is shown in the "Reflow Solder" drawing in Figure 2.

The physical structure of the solder after the plating step is therefore altered during the reflow step to produce the ground interconnect shown in the Cowles patent. This method is very different from the invention, where the plating process effectively forms the interconnect. To more particularly point out and distinctly claim this feature, claim 1 is amended to recite that the plated interconnect has the physical structure of the conductive material as electroplated. This feature distinguishes the claimed process from that disclosed in the Cowles patent. By effectively eliminating the need for the reflow step, the claimed invention provides a more efficient method for making interconnects.

The Rinne patent discloses a method for forming solder bumps on integrated circuit substrates. During the step referred to in the Office Action and described in connection with Figure 1F, the solder bumps (30) are electroplated onto a wetting layer (28) in the openings of a plating template (26). Like the process disclosed in the Cowles patent, this electroplating step is an initial step to apply the solder to the desired location. As noted in the first paragraph in column 7 of the Rinne patent, the electroplated solder bumps are then reflowed. In addition to not disclosing a method for forming an interconnect on an integrated lead suspension component, the Rinne patent does not disclose a plated interconnect having the physical structure of the conductive material as electroplated.

For these reasons, claims 1, 7, 10 and 11 recite an electrical interconnect forming process that is neither taught nor suggested by the prior art references of record. Withdrawal of the §103 rejection of these claims is requested.

Claim 6 depends from claim 1 and is patentable for the reasons discussed above. Claim 6 further characterizes the method as one for forming a plated bond pad that is electrically isolated from the conductive lead layer. Neither the Cowles nor the Rinne patents disclose a method for making a bond pad of this type. Withdrawal of the §103 rejection of claim 1 is requested for this additional reason.

Claim 9 depends from claim 7 and is patentable for the reasons discussed above. Claim 9 further characterizes the method as including the step of forming an aperture through the spring metal layer but not the conductive lead layer, and forming a spring metal side interconnect. Neither the Cowles nor the Rinnes patents disclose a method including these steps. Withdrawal of the §103 rejection of claim 9 is requested for this additional reason.

§103 Rejection of Claims 2-5

Claims 2-5 stand rejected under 35 U.S.C.§103 as being unpatentable over the Cowles and Rinne patents and further in view of the Shangguan et al. U.S. Patent 6,082,610. However, claims 2-5 depend directly or indirectly from claim 1 which is patentable for the reasons discussed above. Withdrawal of the §103 rejection of claims 2-5 for at least this reason is requested.

§103 Rejection of Claims 12 and 13

Claims 12 and 13 stand rejected under 35 U.S.C.§103 as being unpatentable over the Cowles and Rinne patents and further in view of the Gay et al. U.S. Patent 4,764,260. The Gay patent is said to teach a method of anodic cleaning of a stainless steel substrate to improve adhesion between the plated layer and the stainless steel. However, these claims depend directly or indirectly from claim 1 which is patentable for the reasons discussed above. Withdrawal of the §103 rejection of claims 12 and 13 for at least this reason is requested.

New Claim 23

By this response new claim 23 is added to the application. This claim depends from claim 1 and further characterizes the electroplating step as electroplating the first conductive material on the spring metal layer at the interconnect site to form an electrical interconnect between the spring metal layer and conductive lead layer. A method having these features and associated advantages is neither taught nor suggested by the references of record. Consideration and allowance of claim 23 is requested.

Conclusion

All pending claims 1-7, 9-13 and 23 recite an interconnect forming method that is neither taught nor suggested by the references of record. This method enables the efficient fabrication of a high-quality interconnects. Allowance of these claims is requested.

Respectfully submitted,

FAEGRE & BENSON LLP

By: _____

Walter C. Linder, Reg. No. 31,707
612/766-8801
Customer No.: 25764

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